AD 406 301

SOLID STATE MICROELECTRONICS SYSTEMS

Report No. 2

SC Contract No. 36-039 AMC-00020

Second Quarterly Progress Report

1 December 1962 to 1 March 1963

U.S. ARMY ELECTRONICS RESEARCH AND
DEVELOPMENT LABORATORY
FORT MONMOUTH, NEW JERSEY

GENERAL ELECTRIC COMPANY
HEAVY MILITARY ELECTRONICS DEPARTMENT
SYRACUSE, NEW YORK

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Report Prepared by

G. Danielson
R. Marolf
R. Warr

Electronics Laboratory
GENERAL ELECTRIC COMPANY
Syracuse, New York

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I. PURPOSE

The purpose of this contract, as outlined in technical requirements for PR and C No. 63-ELP/R-4500, is to carry out studies leading to specific information and criteria which can be used in evaluating the potential merits and limitations of various approaches to microelectronics. Effort will be applied to theoretical and experimental analysis of microelectronics and to an investigation of state of the art hardware.

The program is divided into two phases as follows:

Phase I - The Phase I effort consists of theoretical and an experimental analysis in the following specific areas:

Power Dissipation - Studies on the minimum power level at which circuits can be operated satisfactorily will continue. Emphasis will be given to the determination of projected improvements in low level active devices and novel circuitry approaches.

Reliability - The various effects of component tolerances or device variations on systems of circuits will be determined. Studies will be conducted to determine the proper level of integration to be achieved for the various microelectronic forms. Studies of redundancy will be made and investigations conducted to determine the ecomonic feasibility of redundancy techniques. The interconnecting problem will be analyzed in relation to the optimum level of circuit integration.

Adjustability - Investigations of electronic self-adjustment of critical circuit parameters will be conducted.

Phase II - The Phase II effort consists of design, fabrication and evaluation of selected portions of hardware. A subassembly consisting of state of the art hardware will be constructed and evaluated. A number of digital filters will be designed, constructed and evaluated.

II. ABSTRACT

The paper design for the Digital Data Terminal AN/TYC-1 (XC-2) has been completed. Detailed logic diagrams for the major portion of the Terminal based on Texas Instruments Solid Circuits and Fairchild micrologic elements are presented.

A microelectronics study for the Telegraph-Telephone Terminal AN/TCC-29 has been initiated. The application of microelectronic techniques to the complete AN/TCC-29 will be studied, but initial efforts have been limited to an evaluation of possible digital filter applications within this equipment. The use of both passive RC and active RC networks within a digital filter is considered.

III. CONFERENCES AND REPORTS

A. CONFERENCES

a) Date: 9 January 1963
Place: USASRDL, Fort Monmouth, New Jersey
In Attendance: J. Hohmann, USASRDL
A. Bramble, USASRDL
J. Raper, E. Lab., General Electric Company
G. Danielson, E. Lab., General Electric Company
R. Marolf, E. Lab., General Electric Company
R. Warr, E. Lab., General Electric Company
J. Newsom, HMED, General Electric Company
Subject: Program Review and Discussion of Some Changes in the Program Effort.

b) Date: 28 February 1963
Place: USASRDL, Fort Monmouth, New Jersey
In attendance: J. Hohmann, USASRDL
A. Bramble, USASRDL
R. Farley, USASRDL
J. Raper, E. Lab., General Electric Company
G. Danielson, E. Lab., General Electric Company
M. Clark, SPD, General Electric Company
Subject: Discussion On Program Effort.

B: REPORTS

a) Monthly Letter Report No. 2 (1 December 1962 to 31 December 1962)

b) Monthly Letter Report No. 3 (1 January 1963 to 31 January 1963)

IV. FACTUAL DATA

A. MICROELECTRONIC SYSTEM DESIGN

1.0 Introduction

The objectives of this portion of the contract have been redirected during the last quarter. The Digital Data Terminal study has been concluded and a study on a new equipment, the Telegraph-Telephone Terminal AN/TCC-29 has been initiated.

A paper design based on Texas Instruments Solid Circuits and Fairchild micrologic elements has been worked out for the major portion of the Digital Data Terminal Transmitter and Receiver. Special emphasis was placed on design details such as module count, power consumption, design flexibility, etc. No attempt was made, however, to use standard digital modules to the largest extent possible.

A similar study will be conducted for the Telegraph-Telephone Terminal AN/TCC-29. The existing equipment comprises LC band pass filters of considerable size and weight; an evaluation presented in section 3 indicates, that these filters may be replaced advantageously by microelectronic digital filters.

2.0 Digital Data Terminal AN/TYC-1(XC-2)

The block diagram of the Digital Data Terminal AN/TYC-1(XC-2) Transmitter has been shown and briefly discussed in the first quarterly report. For reference, it is shown again in Figure 1, and the block diagram of the Receiver is represented in Figure 2.

Detailed logic diagrams have been worked out and will be described in this section for the following blocks:

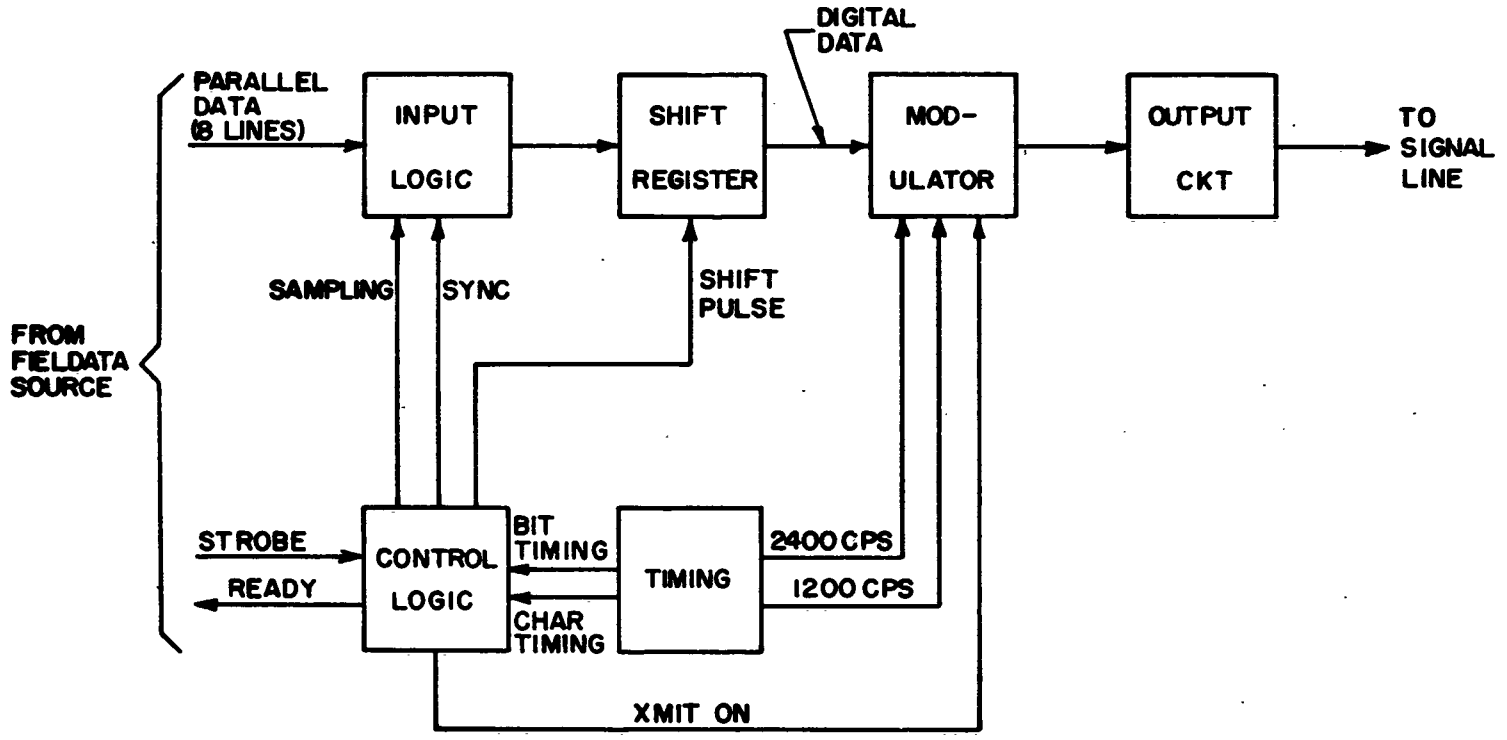
Transmitter: Input logic, shift register, control logic and timing unit (except for oscillator).

Receiver: Serial register, output register, timing unit (except for oscillator), character sync., control logic (except for signal detector) and data detector (except for integrator).

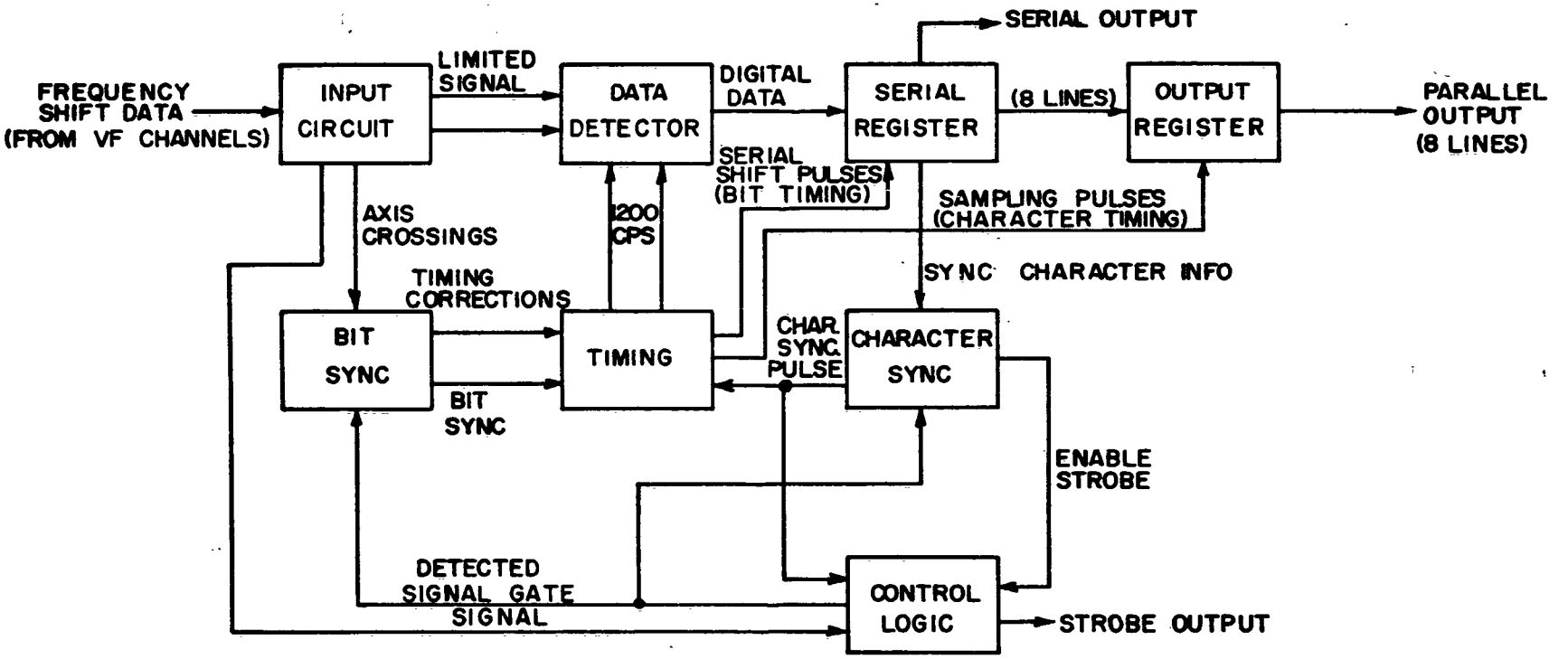
All these blocks perform strictly digital functions and the existing diagrams can therefore be converted in a rather straight forward manner to be compatible with either the Texas Instruments Solid Circuits family or with the Fairchild micrologic modules.

The building blocks listed above comprise the major portion of the Data Terminal. There are, however, certain functions left which cannot be realized with strictly digital modules. Among these functions are: tuned amplifiers, output amplifier (linear), delay equalizer, signal detector, stable oscillators, etc.

No attempt was made to use standard digital modules to the largest extent possible since a practical solution more likely consists of a combination of standard modules with special circuits designed either as thin film, integrated, or modular microelectronics building blocks. Certain functions can be performed by combining the standard logic building blocks with external components. Blocking oscillators, for instance, may be replaced by inverters (NOR gates) with proper RC networks connected to the inputs. The same configuration may be used in place of a monostable delay multivibrator.



TRANSMITTER BLOCK DIAGRAM
FIGURE 1



RECEIVER BLOCK DIAGRAM

FIGURE 2

Special consideration was given to functions performed by LC tuned circuits in the original design. The Digital Data Terminal employs two LC tuned amplifiers, one tuned to 1200 cycles and the other tuned to 2400 cycles. Each amplifier is driven by a square wave at the frequency to which the amplifier is tuned, and the amplifier produces a sinusoidal output at the square wave frequency.

Conventional LC tuned amplifiers are generally incompatible with microelectronic techniques becasue of the lack of microelectronic inductors. The LC tuned amplifiers could be replaced with microelectronic active RC filters, but the present conventional amplifiers are rather high Q (about 50) and also employ trimming capacitors for phase adjustment. The fabrication of active RC filters to duplicate this performance would be quite difficult and may not be worthwhile. However, with modest reductions in the amplifier performance, the active RC filter fabrication difficulties can be eased considerably. For example, components trimmed to 1% could yield a filter with a Q of 20 and a phase shift of less than 10^{0}.

Tuned LC networks are also used in the delay equalizer to provide the desired phase compensation. Here again, this function could be performed by an active RC filter in microelectronic form.

While some logic functions such as counters, shift registers and pulse generators have been realized using Texas Instruments Solid Circuits, the detailed logic diagrams shown in Figures 3 to 19 represent a paper design. They form the base for a discussion of the potential merits of the two integrated circuit families in digital communication equipment in terms of component count, power dissipation, number of cans, etc. They do not allow, however, any conclusions as to noise immunity, margins on supply voltages, etc. and incorporate the manufacturer's specifications for temperature range, fan power, etc.

Before going into the details of individual blocks, the following general remarks can be made about the two circuit families from a logic designer's viewpoint.

Both families are based on NOR (NAND) logic. Besides the basic NOR gate, both families offer various combinations of these gates. In general, however, Solid Circuits have higher fan power than micrologic elements. In an extreme example found in the character sync. circuit of the receiver, 7 micrologic G elements or 2 Solid Circuits SN512 were required to perform the NOR function of 12 inputs. Fan-out power is also somewhat higher for Solid Circuits and the optional emitter follower output on the NOR gate and the flip-flop was found to be very convenient.

The NOR gates of both families can be operated as pulse generators or delay "monostables" by connecting the input through a resistor to the positive bias voltage and by coupling the input capacitively. For the Solid Circuits, both resistor and capacitor are external components, while the micrologic element B requires only an external capacitor. A negative transition at the input generates a positive output pulse, whose duration can be varied over a wide range by choosing the proper RC time constant.

Logically, the main difference between the two circuit families lies in the flip-flop, and here the Solid Circuits flip-flop is definitely more versatile. Since the micrologic system does not use capacitors at all, its flip-flop has no "built-in" memory. Thus, counters and shift registers require two half shift register elements per stage and memory is provided by a 2 phase clock (whereby the second clock phase can be generated internally). A second complication occurs when a flip-flop consisting of 2 half shift registers has to be set. In this case, a third element (C) is required. A typical micrologic counter stage consists therefore of 3 elements and consumes 225 mW while a single Solid Circuits flip-flop (SN510) performs the same function consuming 2 to 8 mW. The fact that the micrologic flip-flop is faster than the Solid Circuits flip-flop is of no advantage for the application under discussion. The Solid Circuits flip-flop is set by a voltage transition while the micrologic flip-flop is set by a voltage level. Using a voltage transition provides some design flexibility which was found to be quite convenient; it allows

the flip-flop to be triggered either at the leading edge of a negative pulse or at the trailing edge of a positive pulse. This flexibility might be bought, however, at the price of higher noise sensitivity.

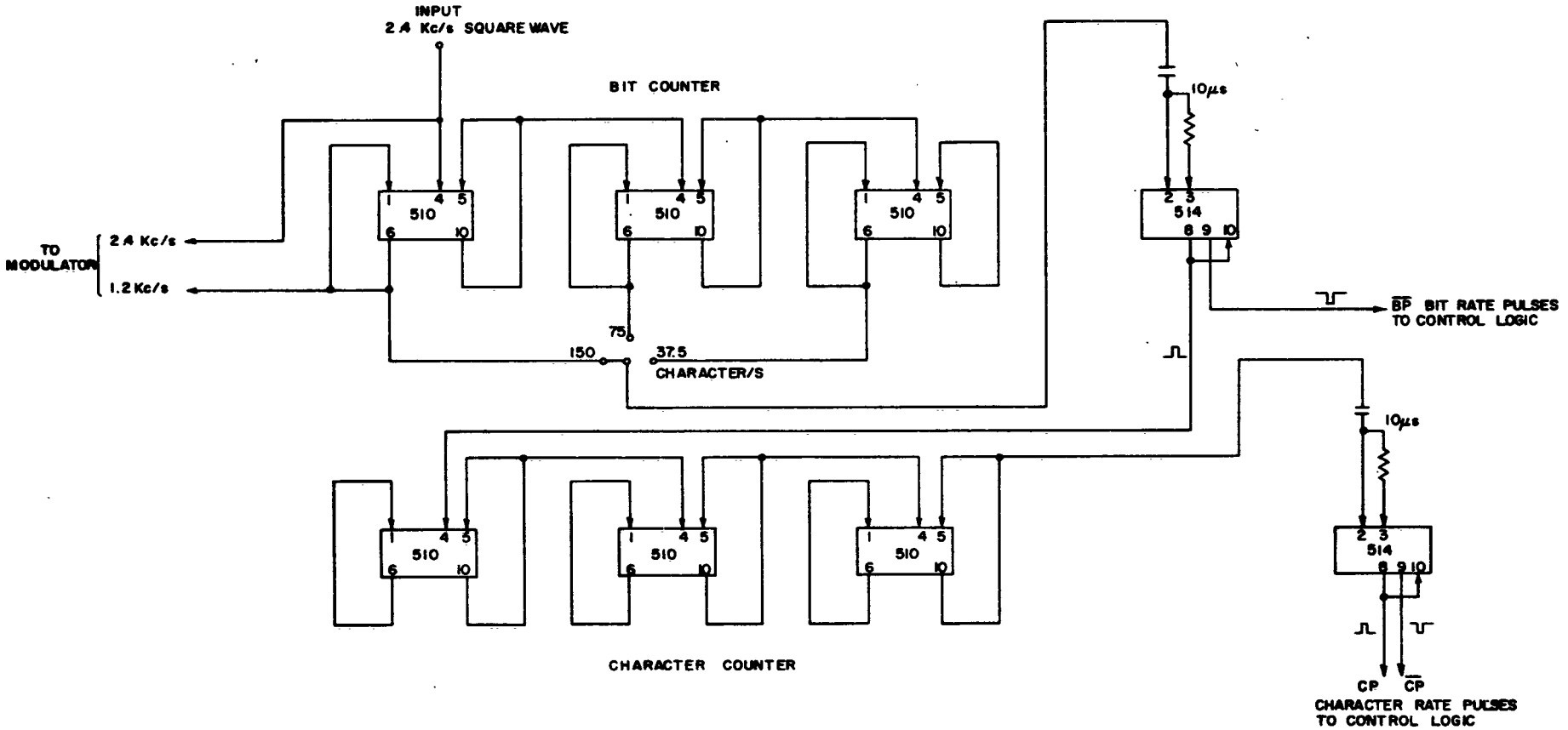
The following remarks may be helpful in interpreting the diagrams on the following pages:

The Transmitter and the Receiver have been split up in the same blocks as shown in Figures 1 and 2. These blocks perform the same functions as in the original design and an attempt was made to draw the diagrams in a manner that they can easily be compared with the corresponding diagrams in the Technical Manual of the existing equipment. Description of the diagram will be included only where they differ considerably from the original ones. The states of the flip-flops in the control circuits during standby, mode switch on "operation", are indicated in the diagram. Positive logic is used throughout (high voltage logic one, low voltage logic zero). Where an RC network is used in conjunction with a Solid Circuits gate or an R in conjunction with a micrologic B element, the pulse width is indicated. The symbols for cans or modules are used rather than logic symbols for gates and flip-flops. It is assumed that all leads number 3 are connected to $+V_{cc}$ and all leads number 7 to ground for the Solid Circuits, while all pins number 8 are connected to $+V_{cc}$ and all pins number 4 to ground for the micrologic elements. Exceptions in both cases are the combined NOR gates.

2.1 Transmitter

2.1.1 Timing Unit (Figure 3 and 4)

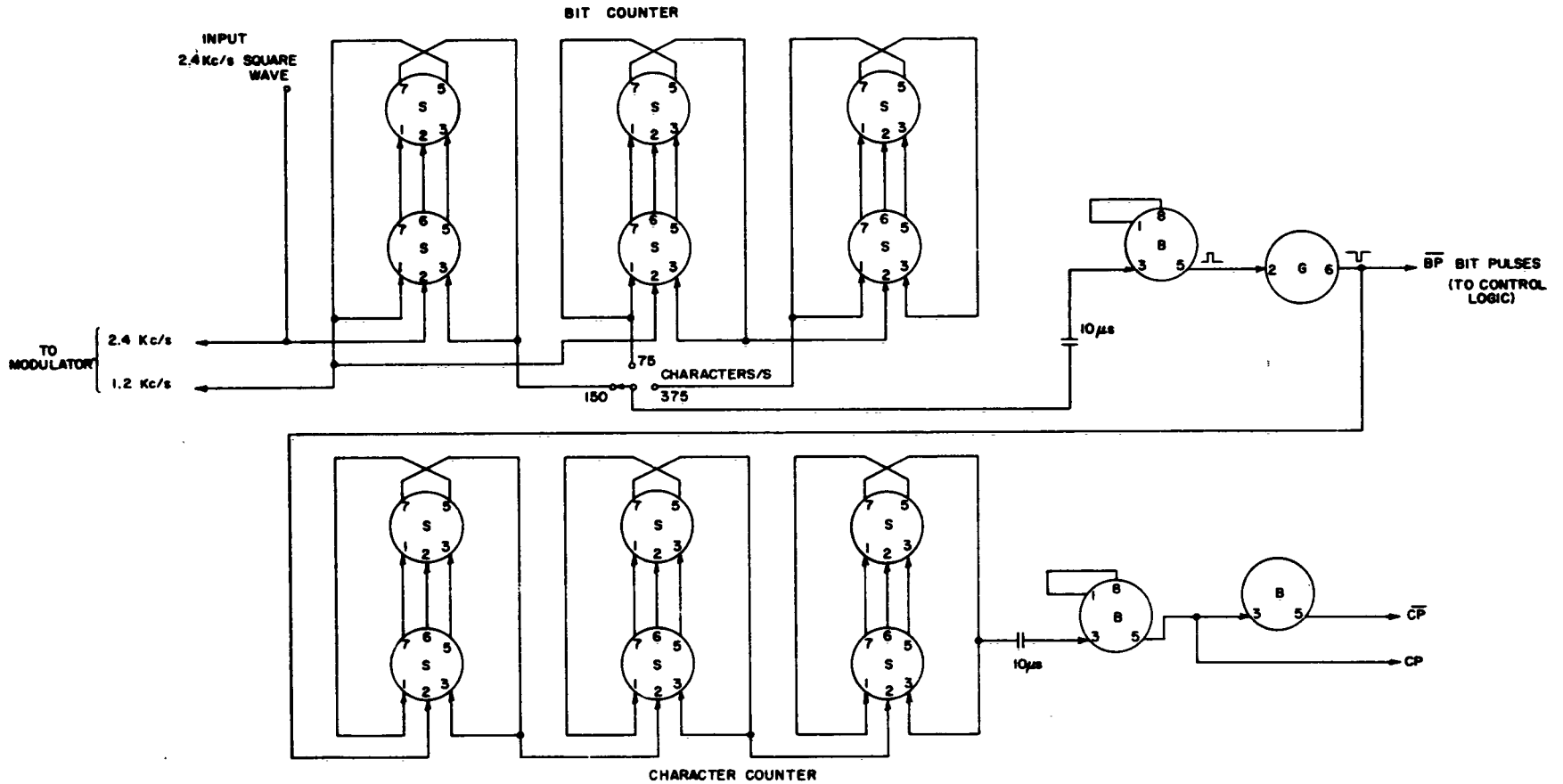
The timing units shown in Figure 3 (Solid Circuits) and Figure 4 (micrologic) do not include the 2.4 kcs square wave generator. A tuning fork oscillator may be used as in the original design or the 2.4 kcs frequency may be derived from the crystal controlled oscillator used in the Receiver.



NOTE: CP APPEARS IMMEDIATELY AFTER $\overline{BP}$ (SINCE THE TRAILING EDGE OF BP TRIGGERS THE CHARACTER COUNTER)

TRANSMITTER, TIMING UNIT, SOLID CIRCUITS

FIGURE 3



NOTE: CP AND $\overline{CP}$ APPEAR IMMEDIATELY AFTER $\overline{BP}$ (SINCE POSITIVE TRANSITION OF OUTPUT FROM G TRIGGERS CHARACTER COUNTER)

TRANSMITTER, TIMING UNIT, MICROLOGIC
FIGURE 4

Solid Circuits

Each counter stage requires one SN510 module. The output of the bit rate counter is applied to an SN514 dual NOR gate, the first capacitively coupled gate generating positive bit pulses, and the second gate, used as an inverter, generating negative bit pulses of approximately 10 μs width. The trailing edge of the positive bit pulse triggers the character rate counter. Character pulses are generated in the same manner as bit pulses. They occur immediately after the bit pulses.

Micrologic

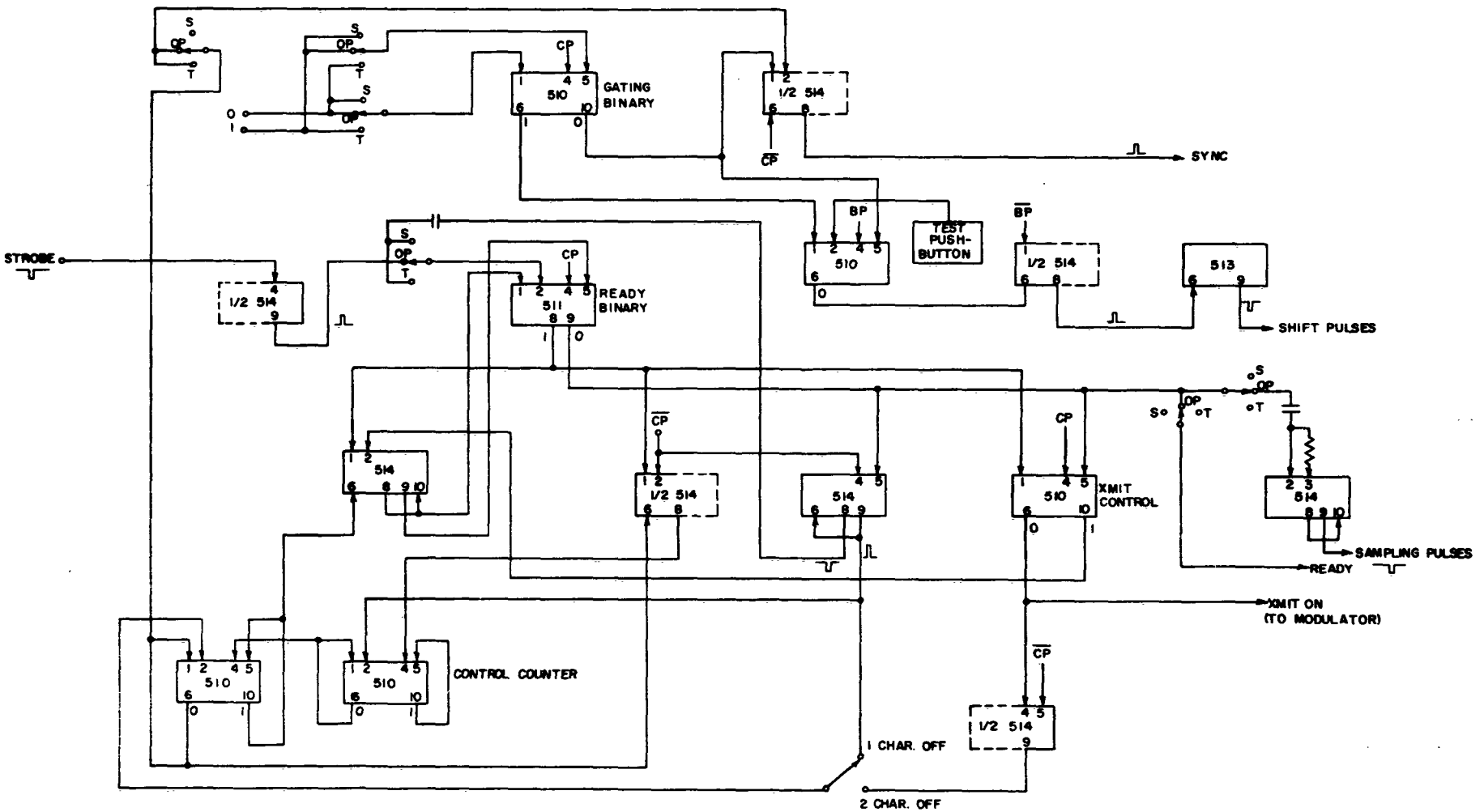
Two S elements are used per counter stage. Again, bit and character rate pulses are generated by capacitively coupled B elements. The bit rate pulses are inverted and the trailing edge triggers the character rate counter, assuring that character rate pulses follow bit rate pulses.

2.1.2 Control Logic (Figure 5 and 6)

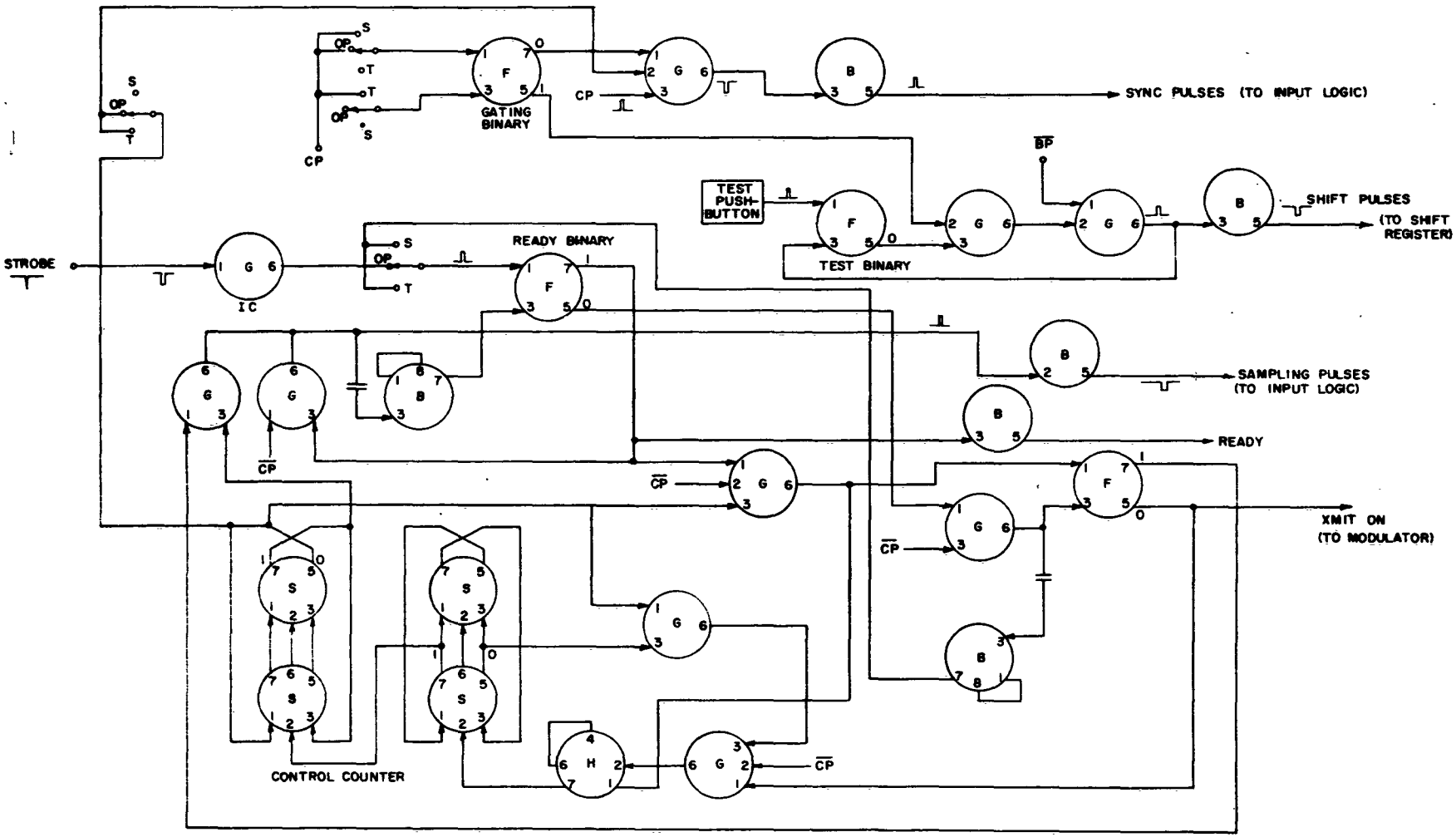
The AND-OR logic shown in the original diagram was replaced by NOR logic using the identities $AB = \overline{A} \downarrow \overline{B}$ and $A + B = \overline{A \downarrow B}$. Further changes were necessary due to the different logic properties of the Solid Circuits and micrologic flip-flops.

In both diagrams, sync. characters are generated slightly differently than in the original diagram. Rather than gating a square wave to the sync. output during the first two character times, two sync. pulses are now generated at the beginning of the first and second character time preceeding data transmission. These sync. pulses set stages 1, 2, 3, 4 and 7 of the shift register (see Figure 7 and 8). Once data transmission starts, sync. pulses are inhibited by the second stage of the control counter.

Assuming that the logic circuits are biased between 0 and -3 v, no output converter may be required for the "ready" output (depending on the loading), while the input converter for the "strobe" input can be



TRANSMITTER, CONTROL LOGIC, MICROLOGIC
FIGURE 5



TRANSMITTER, CONTROL LOGIC, MICROLOGIC
FIGURE 6

replaced by an inverting NOR gate.

Blocking oscillators have been replaced by NOR gates or B elements in conjunction with external R or RC components.

Solid Circuits

The Solid Circuits flip-flop changes states according to dc levels applied to the set and reset input upon a negative voltage transition at the clock pulse input, while the flip-flops used in the original design are triggered by negative voltage transitions applied directly to the set and reset inputs. The original diagram has been changed to be compatible with the logical properties of the Solid Circuits flip-flop.

Micrologic

The following arrangement was used to set the control counter: two outputs of the control counter are combined in a NOR gate. The output of this gate is combined in a second NOR gate with negative character rate pulses and with the output of the "transmitter on" flip-flop. The output of the second NOR gate is applied (through an OR gate) to the input of the counter. Character pulses will therefore be counted until the counter is in the proper state as indicated in Figure 6. If no strobe pulse is received for a full character length, the Transmitter will go off the air for two character times before sync. character transmission can start again. The option "1 character off"/"2 characters off" is not provided.

Since the F flip-flop is switched by a voltage level rather than by a voltage transition, it is not possible to use leading or trailing edges of character pulses as conveniently as with Solid Circuits or with the original flip-flops. Note for instance, that the reset pulse for the "ready" binary has to be generated in a separate B element.

Buffer elements were required at the "snyc. pulse", the "shift pulse" and the "sampling pulse" outputs due to the low fan-out power of the F and G elements.

2.1.3 Input Logic (Figure 7 and 8)

The input logic is the same for Solid Circuits and micrologic modules. A set pulse is generated in channels 5, 6 and 8 whenever a sampling pulse is generated in the control logic and the data input is a one; in channels 1, 2, 3, 4 and 7 a set pulse is in addition generated by a sync. pulse.

Since data is represented by negative logic in the data source, while the diagrams presented in this report are based on positive logic, no input inverters will be required; the negated data inputs shown in Figure 7 and 8 are the actual outputs of the data source. Again, it is assumed that the logic modules are biased between 0 and -3 v volts, and input converters have therefore been omitted.

2.1.4 Shift Register (Figure 8 and 9)

The set pulses generated by the input logic set the 8 stages of the shift register at the sampling or sync. pulse time, which immediately follows the shift pulse time. A zero is applied to stage 8 and shifted through the register during the following character time. At the end of the character time all stages are set to zero.

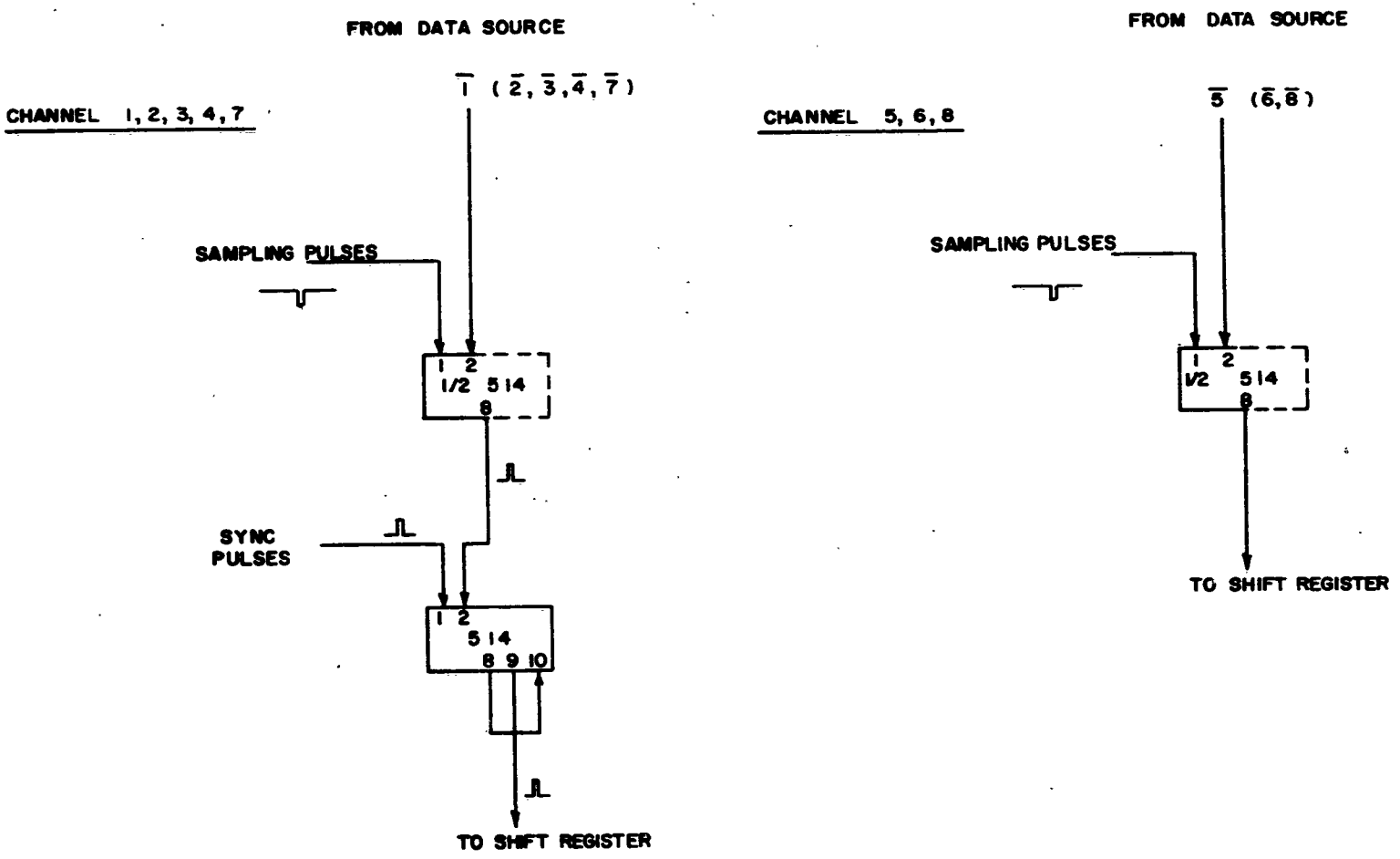
Solid Circuits

One SN511 flip-flop is required per shift register stage. The "preset" input is used to set the stage.

Micrologic

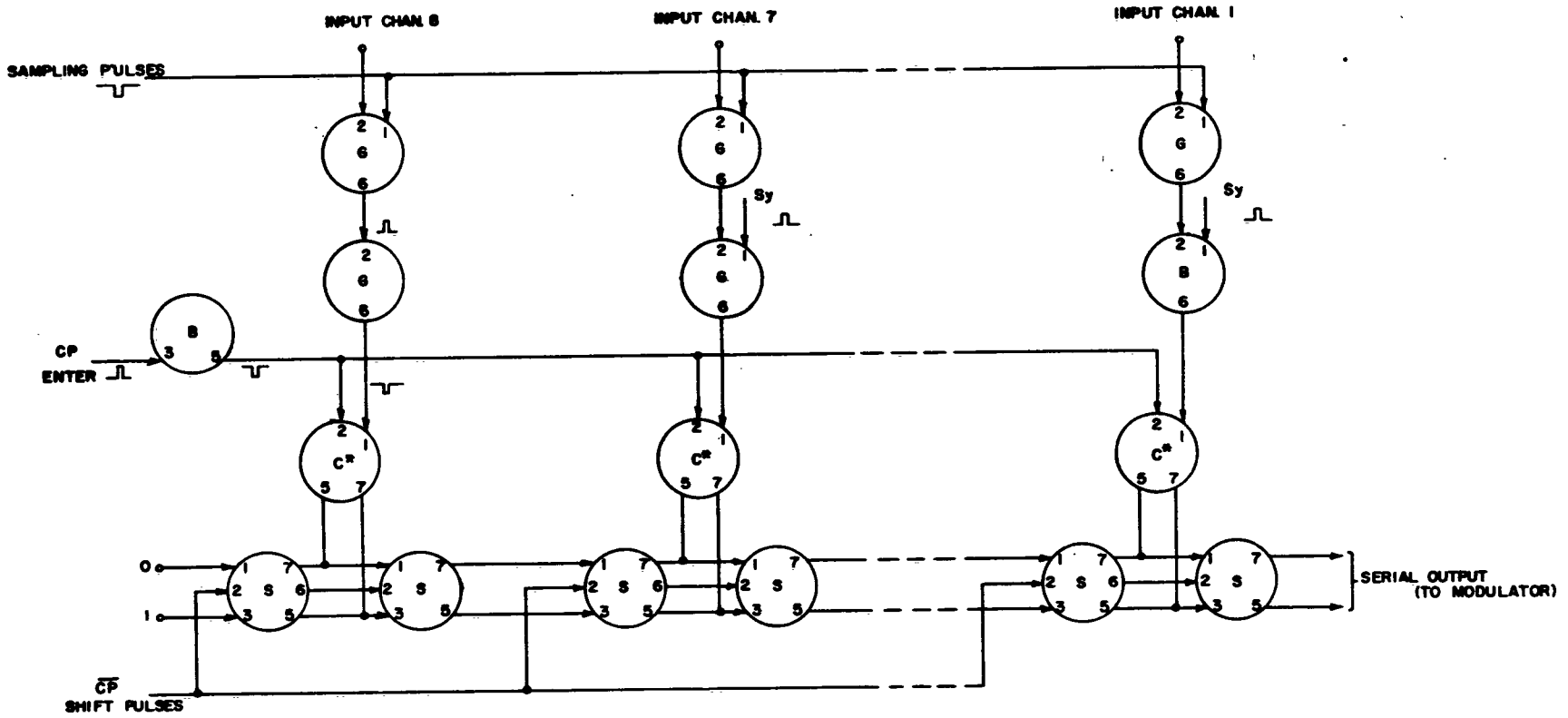
Two S elements and one C element (for parallel read-in) are needed per stage.

2.2 Receiver



TRANSMITTER , INPUT LOGIC, SOLID CIRCUITS

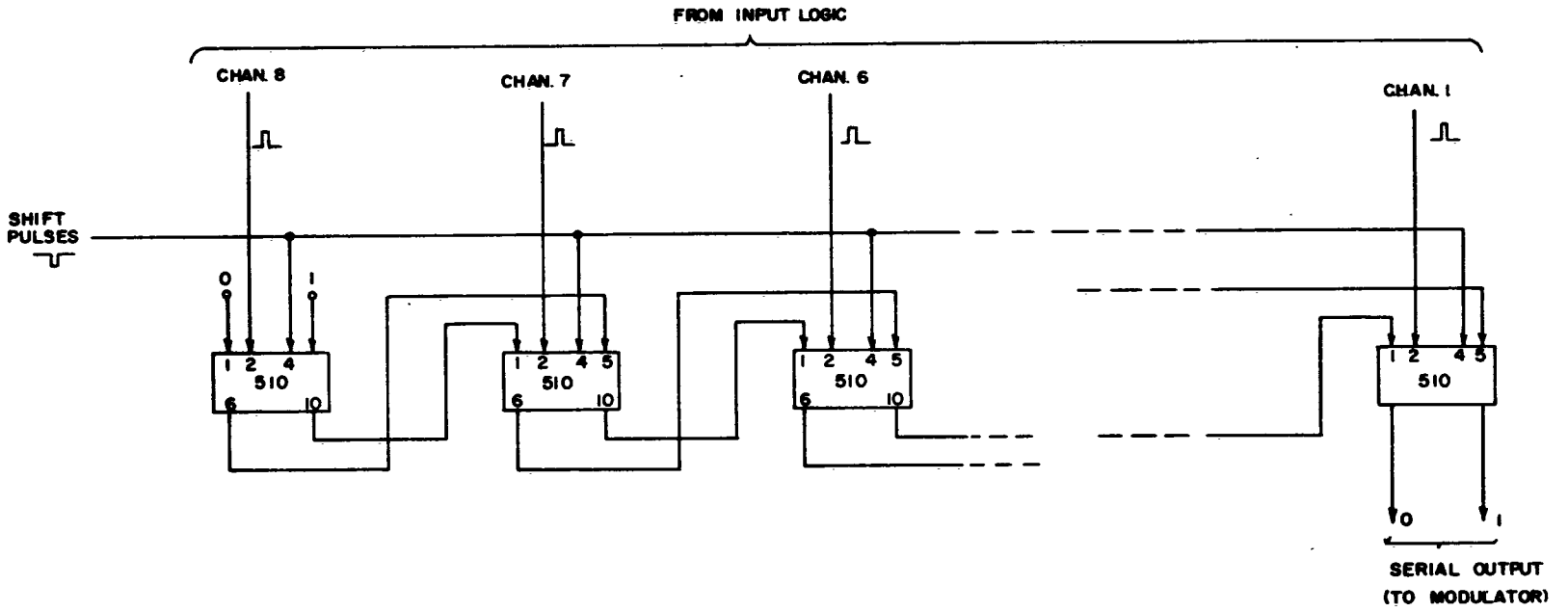
FIGURE 7



* OUTPUT NODE RESISTORS NOT CONNECTED TO $+V_{cc}$

NOTE: "ENTER", "SAMPLING", AND "SYNC" PULSES FOLLOW IMMEDIATELY THE SHIFT PULSES.

TRANSMITTER, INPUT LOGIC AND SHIFT REGISTER, MICROLOGIC
FIGURE 8



TRANSMITTER, SHIFT REGISTER, SOLID CIRCUITS
FIGURE 9

2.2.1 Serial Register and Output Register (Figure 10 and 11)

The serial shift register is fed by the data feed binary and is sampled at the end of each character time. Sampling pulses immediately follow the shift pulses. The content of the serial register is transferred in parallel to the output register, where it is stored for the following character time. Output converters have been omitted again. The logic convention can be made compatible with the data sink, since the actual outputs as well as their negation are available.

Solid Circuits

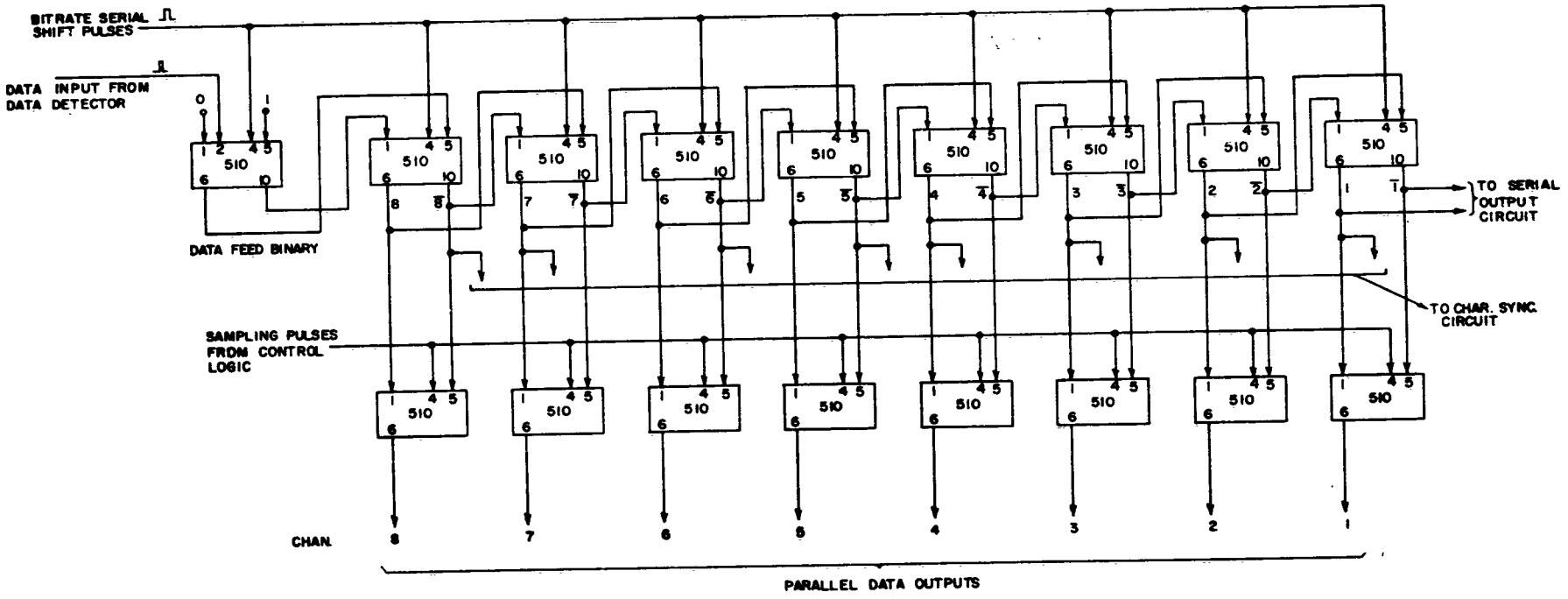
Each stage of the serial and output register consists of one SN510 flip-flop. The data feed binary is set by a positive pulse applied to the "present" input and reset by the shift pulse immediately after having transferred its content to the first serial register stage.

Micrologic

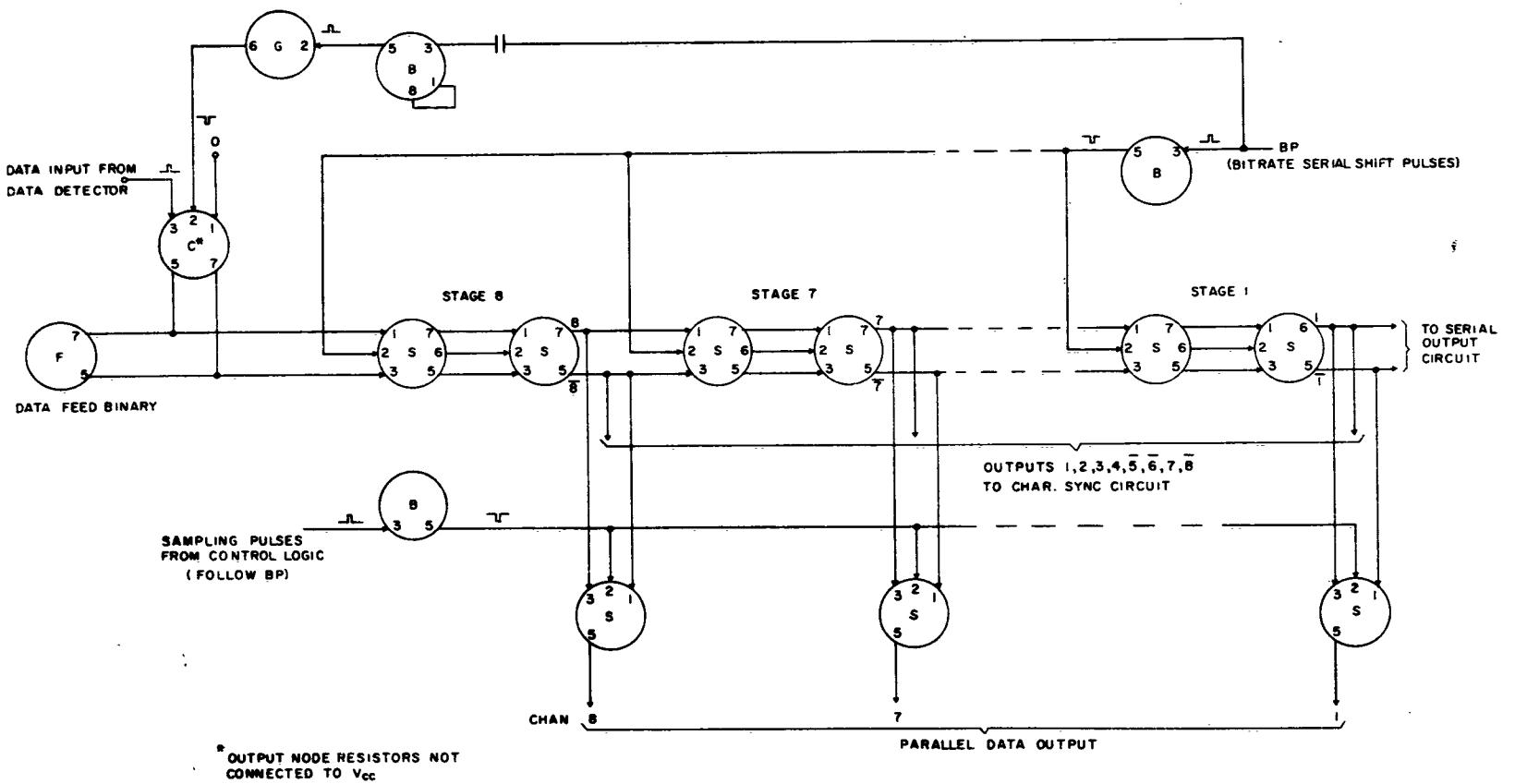
Each serial register stage consists of two S elements, and each output register consists of one S element. The data feed binary consists of a flip-flop which is set and reset through a C element. The "enter" pulse for this element is delayed in a B element pulse generator so that it follows the shift pulses. The data feed binary is therefore reset immediately after having transferred its content to the first serial register stage.

2.2.2 Character Sync. and Control Logic (Figure 12 and 13)

The original diagram can easily be adapted to Solid Circuits or micrologic elements except for the signal detector. The signal detector is represented as a block in the diagram of Figures 12 and 13 and it is assumed that it generates the same output signals upon detection of signal transmission as in the original diagram. The timing of the character, strobe and sampling pulses follows directly from the diagram.

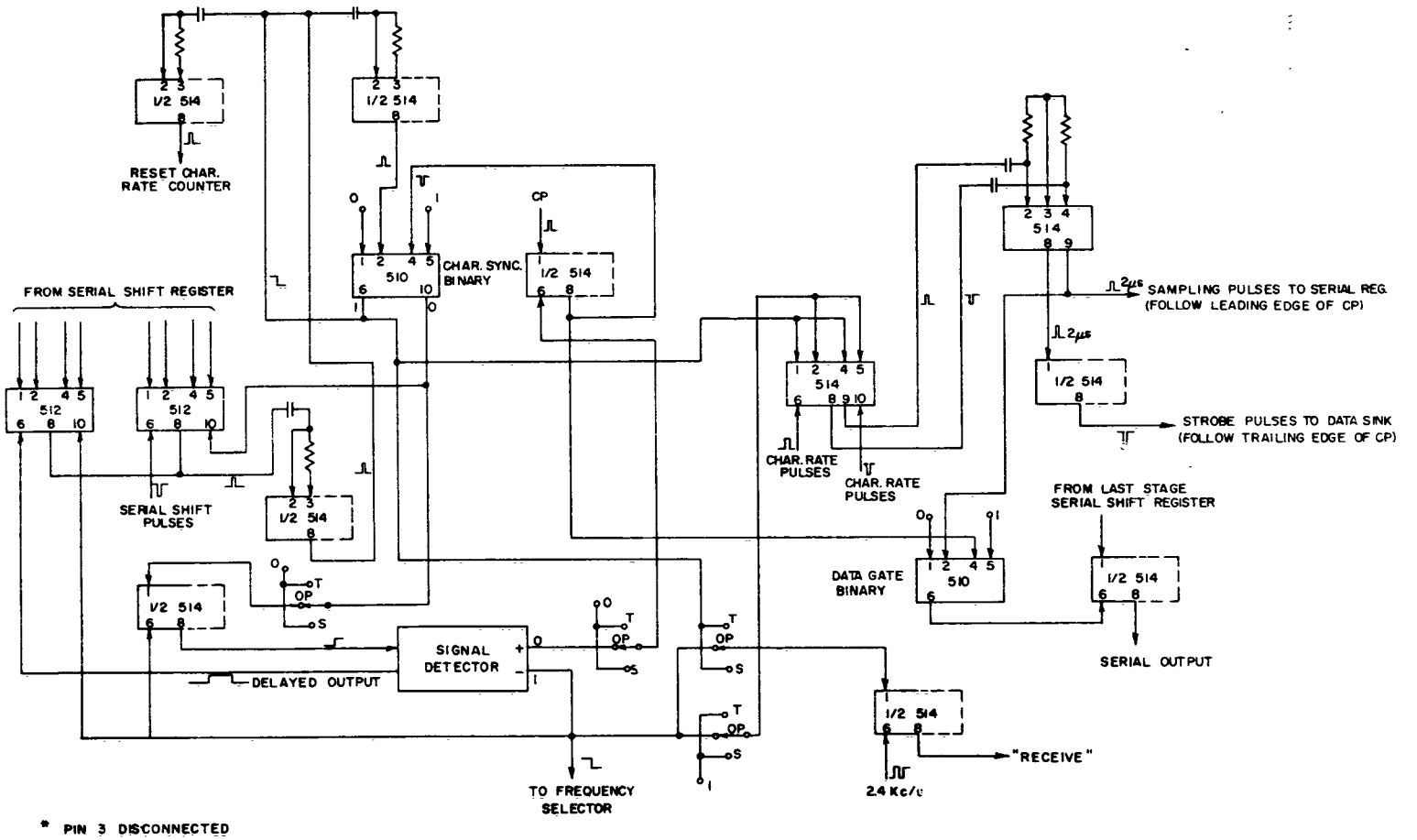


RECEIVER, SERIAL REGISTER AND OUTPUT REGISTER, SOLID CIRCUITS
FIGURE 10



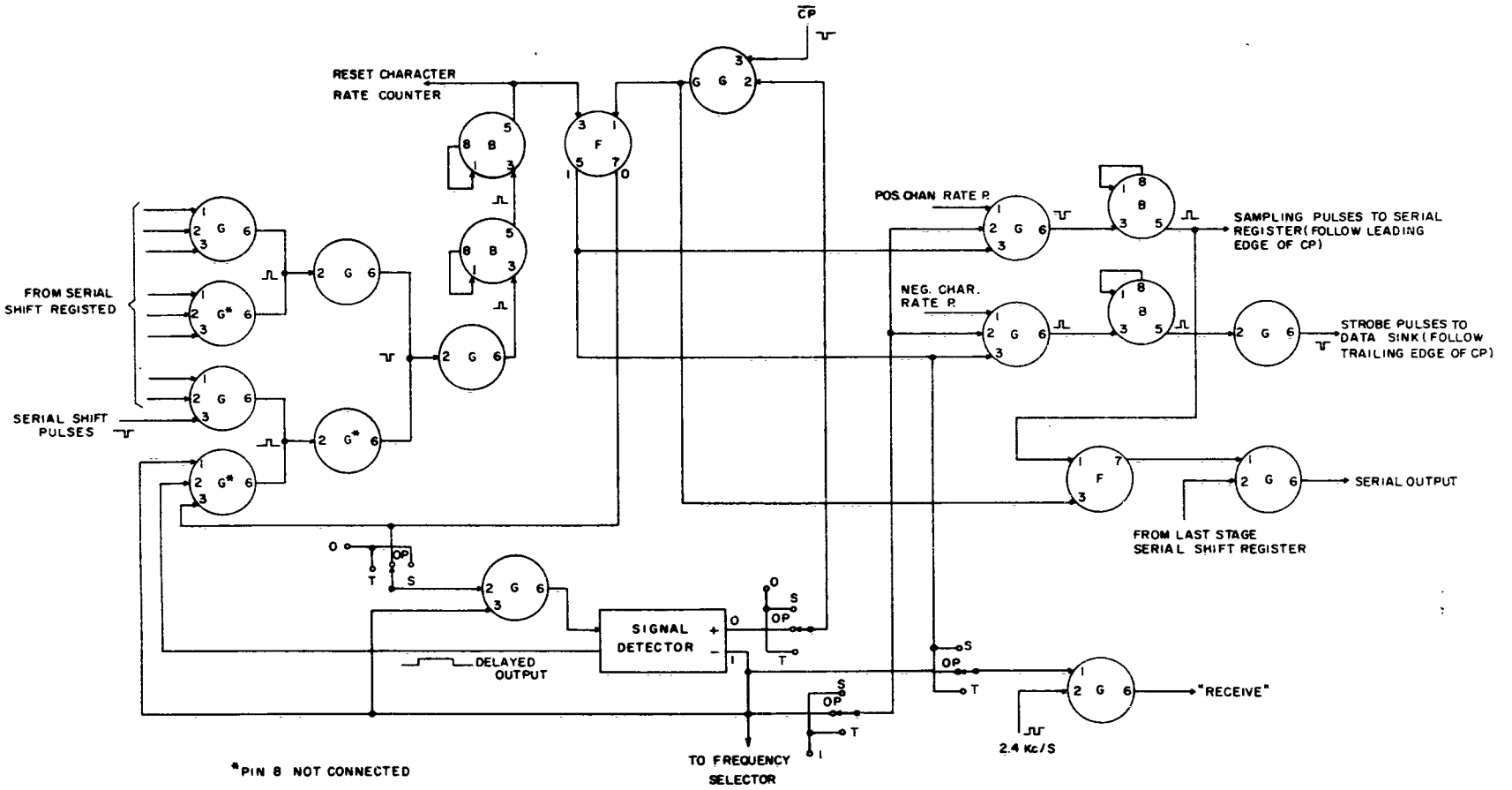
RECEIVER, SERIAL REGISTER AND OUTPUT REGISTER, MICROLOGIC

FIGURE 11



* PIN 3 DISCONNECTED

RECEIVER, CHARACTER SYNC. AND CONTROL LOGIC, SOLID CIRCUITS
FIGURE 12



RECEIVER, CHARACTER SYNC AND CONTROL LOGIC, MICROLOGIC

FIGURE 13

2.2.3 Timing Unit (Figure 14 - 17)

The Solid Circuits and the micrologic version of the add-subtract counter are shown in Figures 16 and 15 and the remaining stages of the bit counter and the character counter are shown in Figure 16 and 17. These diagrams can be compared directly with the original diagram.

2.2.4 Data Detector (Figure 18 and 19)

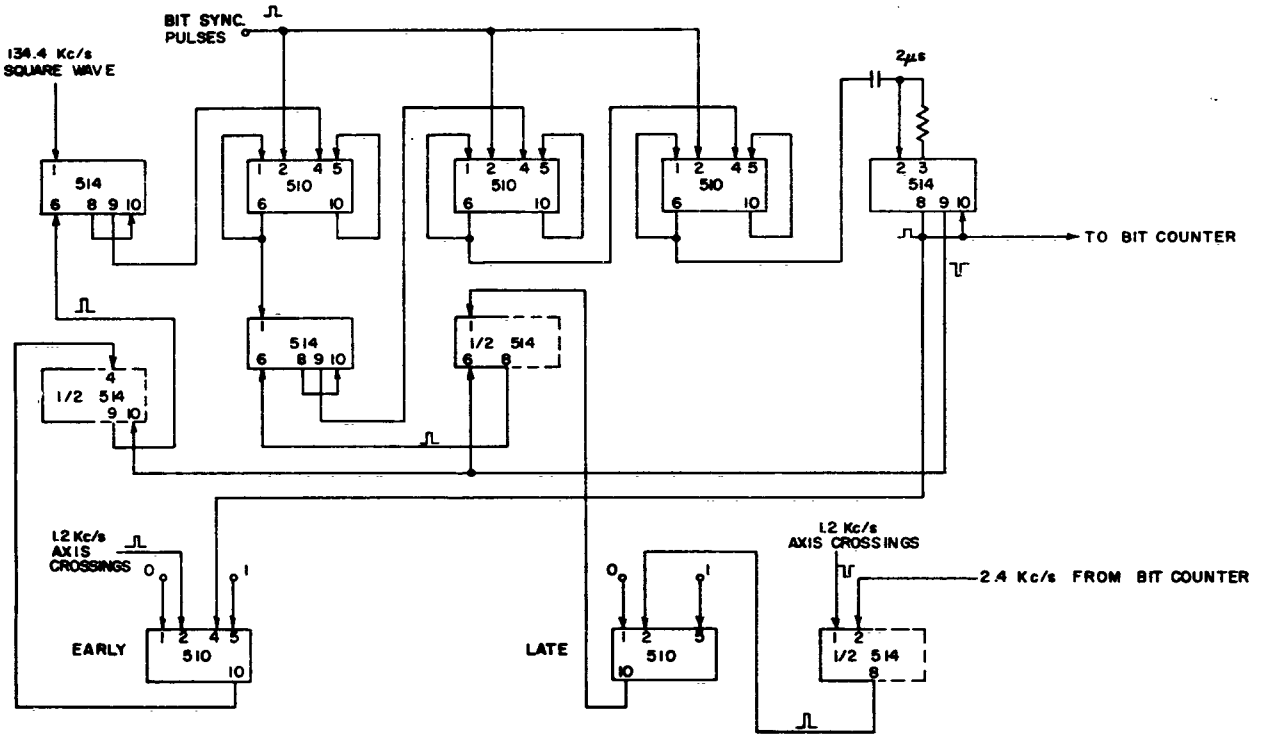
While the integrating circuit in the data detector is not suitable for an adaption to Solid Circuits or micrologic elements, the AND/OR logic can easily be converted to NOR logic.

2.3 Conclusion

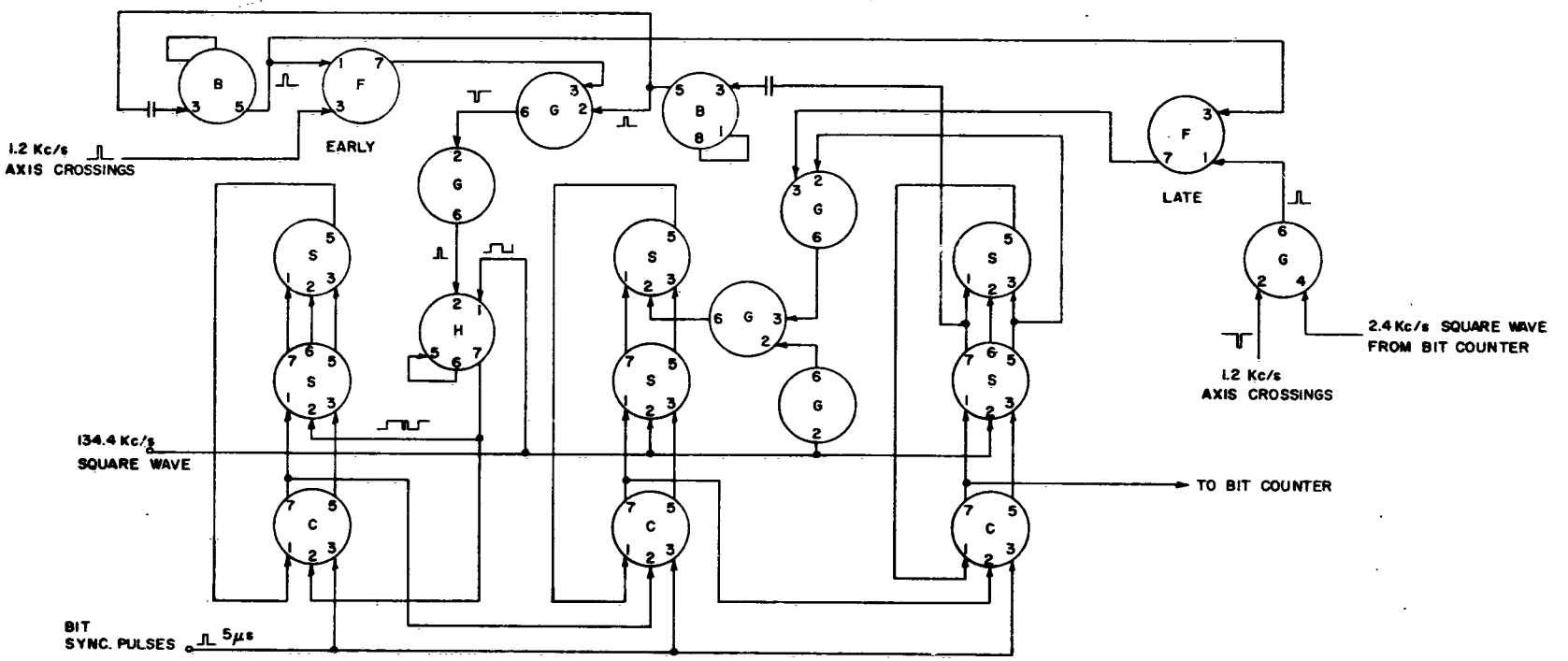
Tables I and II list the number of modules or cans used in the preceeding diagrams and their power consumption. Approximately half as many Solid Circuits will be required than micrologic cans. The total power consumption for the Solid Circuits version is 0.24 W or 0.98 W (for 3 V and 6 V bias voltage resp.) as compared to 8.4 W for the micrologic version.

These numbers are probably not final, but changes which might be found to be necessary in a "debugged" design or possible simplifications will have only little effect. Table II shows, that the heavy power consumers in the micrologic design are the counters and shift registers. A micrologic counter or shift register stage will always require at least two half shift register elements with a total power consumption of 150 mW, while the same functions can be performed with one Solid Circuits flip-flop, consuming 2 to 8 mW.

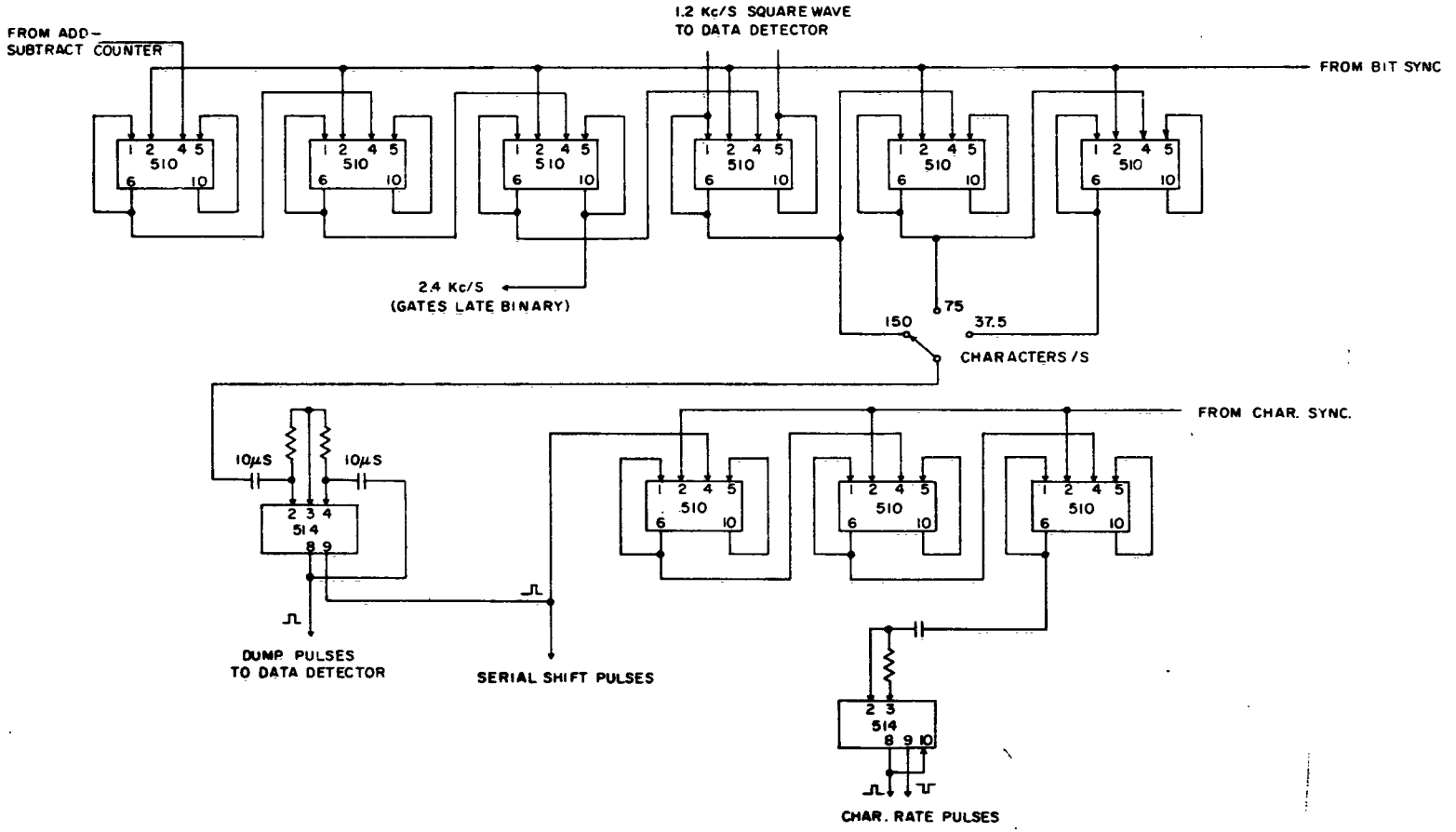
Even though the diagrams presented in this section do not represent the complete Data Terminal, they demonstrate, that a substantial reduction is size, weight and power consumption can be achieved by an integrated electronics version of the present equipment. This is especially true for the Texas Instruments Solid Circuits.



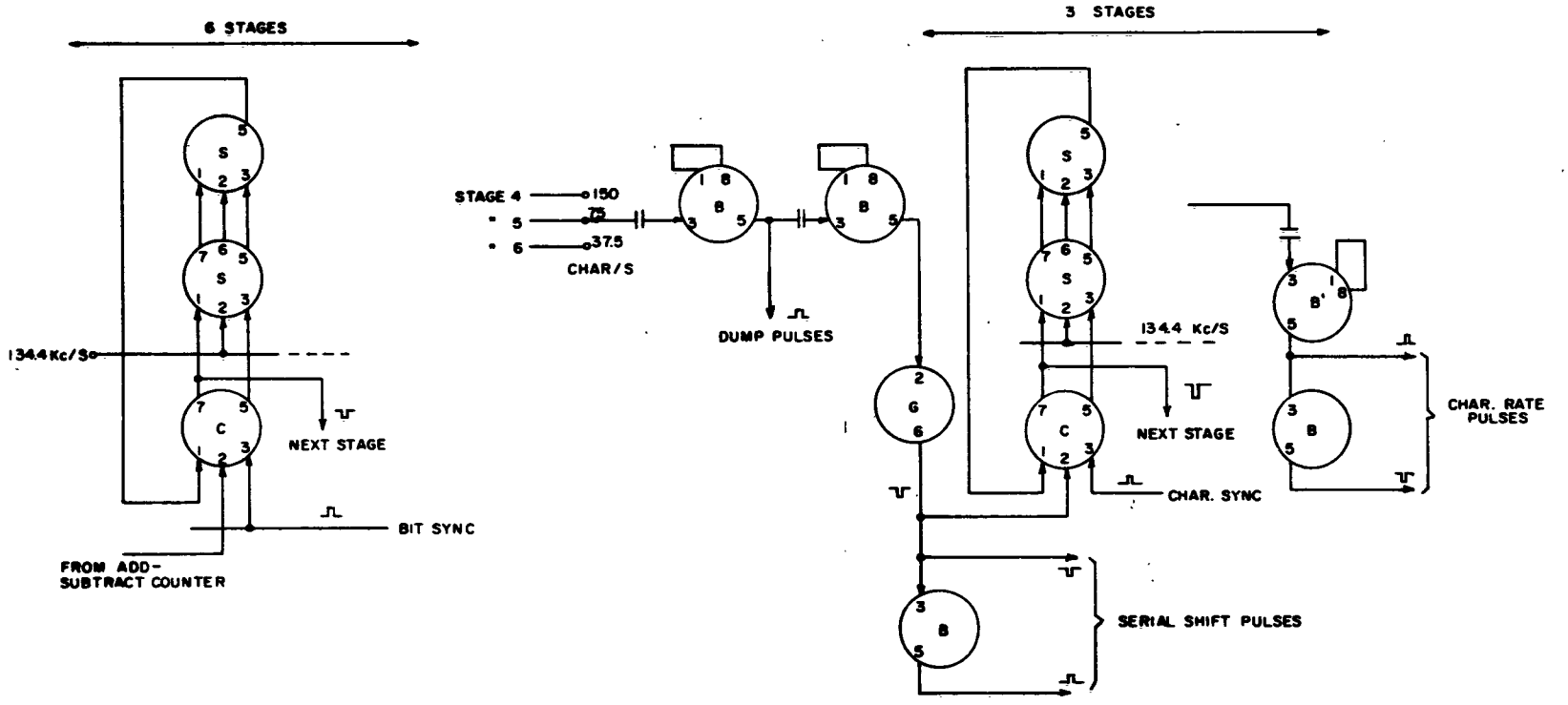
RECEIVER, TIMING UNIT, ADD-SUBTRACT COUNTER, SOLID CIRCUITS
FIGURE 14



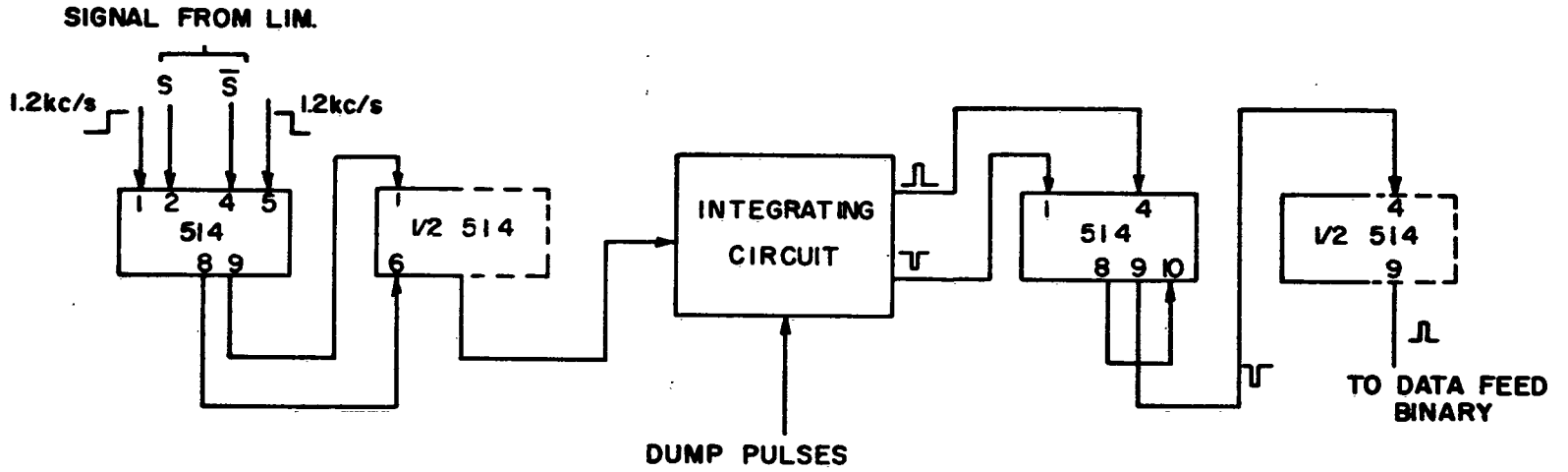
RECEIVER, TIMING UNIT, ADD-SUBTRACT COUNTER, MICROLOGIC
FIGURE 15



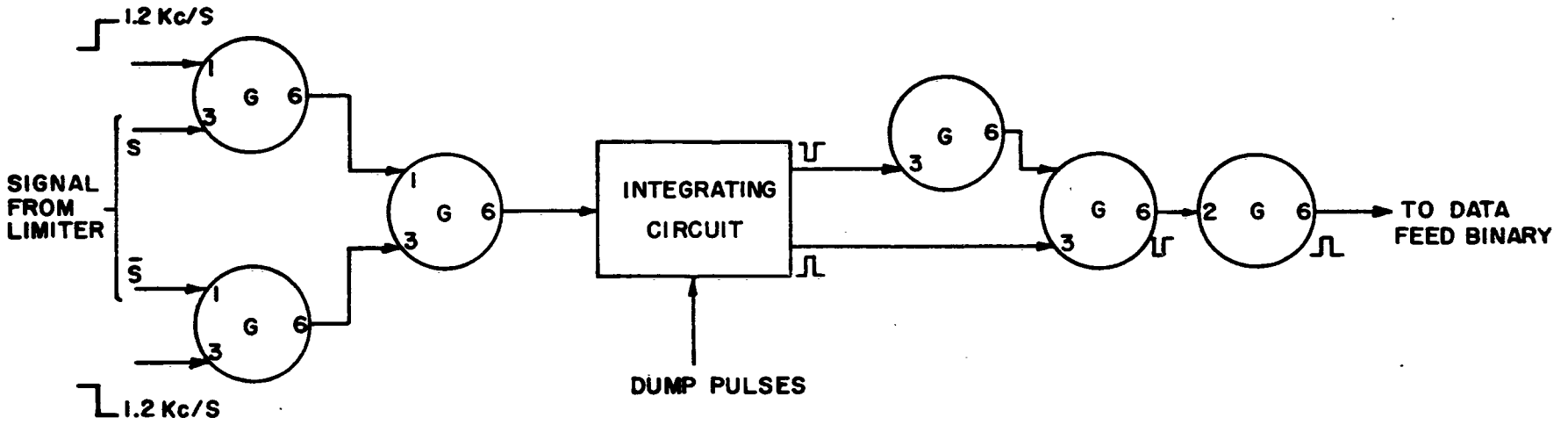
RECEIVER, TIMING UNIT, SOLID CIRCUITS
FIGURE 16



RECEIVER, TIMING UNIT, MICROLOGIC
FIGURE 17



RECEIVER, DATA DETECTOR, SOLID CIRCUITS
FIGURE 18



RECEIVER, DATA DETECTOR, MICROLOGIC
FIGURE 19

	Type	Number	PmW	
			V_{cc} = 3V	V_{cc} = 6V
Transmitter				
Timing Unit:	SN510	6	12	48
	SN514	2	8	32
Control Logic:	SN510	5	10	40
	SN511	1	3	18
	SN513	1	3	13
	SN514	6(5 1/2)	22	88
Input Logic:	SN514	9	36	144
Shift Register:	SN510	8	16	64
		38	110	447
Receiver				
Serial Register a. Output Register:	SN510	17	34	136
Char. Sync. a.:	SN510	2	4	16
Control Logic:	SN512	2	4	16
	SN514	6	24	96
Timing Unit:	SN510	14	28	112
	SN514	7(6 1/2)	26	104
Data Detector:	SN514	3	12	48
		51	132	528
Transmitter and Receiver		89	242	975

Table I. Component Count and Power Consumption for Texas Instruments Solid Circuits

	Type	Number	PmW V_{cc} = 3V
Transmitter			
Timing Unit:	B	3	75
	G	1	15
	S	12	900
Control Logic:	B	6	150
	F	4	120
	G	10	150
	H	1	45
	S	4	300
Input Logic and Shift Register:	B	1	25
	C	8	600
	G	16	240
	S	16	1200
		82	3820
Receiver			
Serial Register a. Output Register:	B	3	25
	C	1	75
	F	1	30
	G	1	15
	S	24	1800
Character Sync. a. Control Logic:	B	4	100
	F	2	60
	G	14	210
Timing Unit:	B	7	175
	C	12	900
	F	2	60
	G	7	105
	H	1	45
	S	24	1800
Data Detector:	G	6	19
		109	4540
Transmitter and Receiver		191	8360

Table II. Component Count and Power Consumption for Fairchild Micrologic Elements

3.0 Terminal, Telegraph - Telephone AN/TCC - 29

3.1 Digital Filter Applications

A preliminary study of the AN/TCC-29 has revealed applications for a digital filter. The Terminal, Telegraph TH-22 (XC-3)/TG contains bandpass filtering which could be performed with a reduction in size and weight by a digital filter. More specifically, the break-in filter (1A1Z2) and the transmitting filter (1A1Z1) provide possible applications for a digital filter. The Filter Assembly F-316/U also provides an application which merits further study. The existing F-316/U is comprised of a bandpass filter and a stopband filter which occupy a volume of 2 1/2 x 10 3/8 x 10 1/4 cubic inches and weigh 12 1/4 pounds. These filters have very rapid cut-off characteristics which appear to be only partially amenable to digital filter techniques. The existing passband filter has a center frequency of 1325 cps and a 3 db bandwidth of about 300 cycles. The attenuation beyond 300 cycles from the center frequency is at least 80 db. The stopband filter has a similar but "inverted" characteristic. The following discussion will be concerned with the ability of a digital filter to approximate these characteristics.

As was shown in an earlier report*, subject to certain constraints, the response function of a digital filter can be viewed as the arithmetic centering of an equivalent lowpass response function about the commutating frequency f_o. The equivalent lowpass response is that of the network shown in Figure 20. The ability to achieve a particular bandpass characteristic from a digital filter therefore depends on whether or not the proper equivalent lowpass response function can be synthesized. Furthermore, from a microelectronics viewpoint, it would be desirable to employ only resistors, capacitors and transistors in the lowpass networks which are incorporated in the digital filter. The digital filters described

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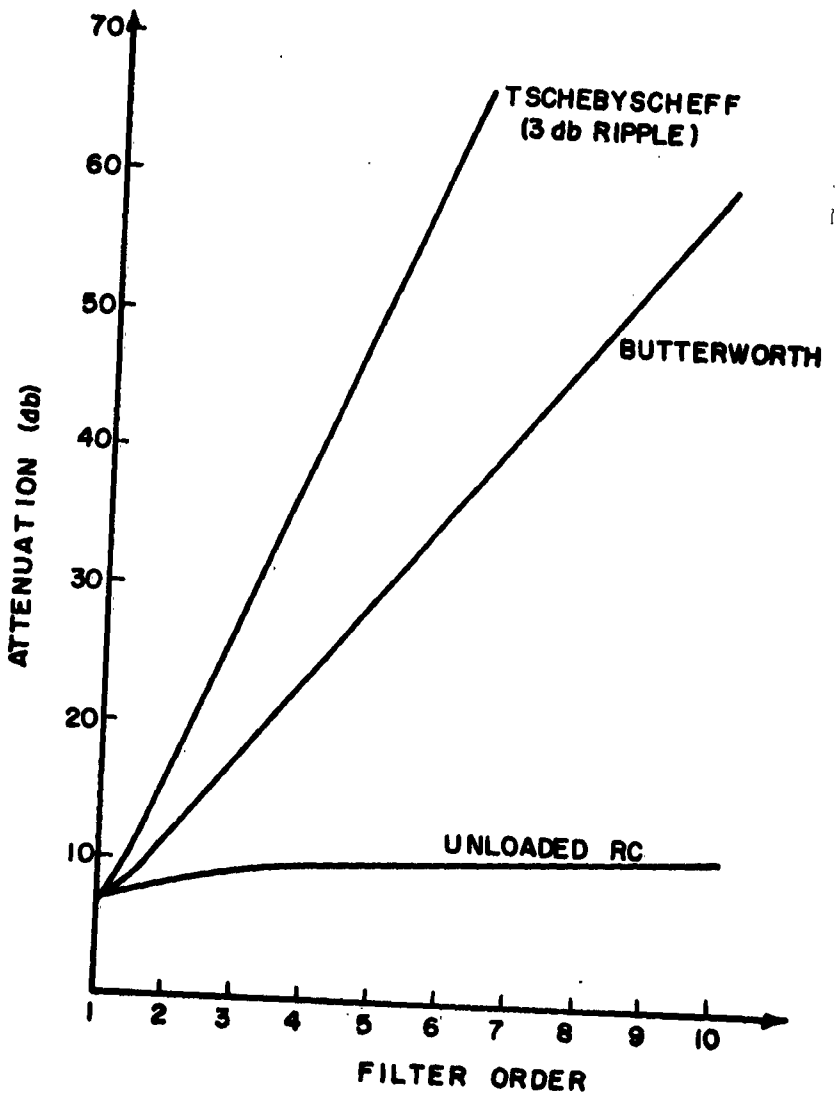
* Third Quarterly Report for SC Contract No. DA-36-039-sc-87466 (Solid State Microelectronics System Program)



LOW PASS FILTER FIGURE OF MERIT
FIGURE 20

in previous reports employed passive RC lowpass networks, but these networks provide very poor approximations to an idealized rectangular transfer function in which the transmission T is

$$T = 1 \quad \text{for } |f| < f_o$$

$$= 0 \quad \text{for } |f| > f_o$$

Active filters which generate either Butterworth or Tschebyscheff characteristics provide much better approximations to the idealized transfer function. The following paragraphs will provide a preliminary assessment of the applicability of these techniques.

3.1.1 Passive RC Lowpass Networks

Digital filters employing passive RC lowpass networks can be readily built, but RC lowpass networks do not possess very sharp cutoff characteristics. A figure of merit which might be applied to a lowpass filter is the following: Let f_o be the frequency at which the lowpass network response is down 3 db. The proposed figure of merit is then the attenuation at 2 f_o. A single RC section has a voltage response of the form,

$$T(jw) = \frac{1}{1 + jw}$$

where the 3 db frequency has been normalized to unity. A straightforward calculation shows that the figure of merit for this filter is then 7 db. If many of these sections are connected in tandem, it might be expected that the figure of merit could be made arbitrarily large, but this is not true. In fact, even if the "round-off" is minimized by assuming no loading on the individual RC sections (this could be approximated by employing emitter followers between sections), the attenuation at 2 f_o is limited to 12 db. This fact can be demonstrated as follows: The response of an N section RC filter (assuming no loading) has the form

$$T(jw) = \frac{1}{(1 + jw)^N}$$

The attenuation can then be written as

$$\alpha = 20 \log (1 + w^2)^{N/2} \text{ db.}$$

For convenience, the frequency is now normalized so the attenuation is 3 db at $\bar{w} = 1$. The normalized attenuation becomes

$$\bar{\alpha} = 20 \log \left[1 + \bar{w} (2^{1/N} - 1)\right]^{N/2} \qquad (1)$$

where the transformation

$$\bar{w} = \frac{w}{\sqrt{2^{1/N} - 1}}$$

has been applied. The attenuation one octave above the 3 db frequency is found by setting $\bar{w} = 2$ in Equation (1) which can then be written

$$\bar{\alpha} (2f_o) = 10 N \log \left[1 + 4(2^{1/N} - 1)\right]$$

$\bar{\alpha} (2f_o)$ is a monotonically increasing function of N, but the function can be seen to asymptotically approach 12 db by applying L'Hospital's rule, i.e.

$$\lim_{N \to \infty} \bar{\alpha} (2 f_o) = \lim_{N \to \infty} \frac{10 \log \left[1 + 4(2^{1/N} - 1)\right]}{1/N}$$

$$= \lim_{N \to \infty} \frac{\frac{d}{dN} 10 \log \left[1 + 4(2^{1/N} - 1)\right]}{\frac{d}{dN} \frac{1}{N}}$$

$$= \frac{40 \ln 2}{\ln 10} \text{ db}$$

$$= 12 \text{ db}$$

The preceding result indicates that a tandem connection of simple RC sections cannot be used when the attenuation one octave above the 3 db cutoff frequency is required to be greater than 12 db.

This same figure of merit can also be applied to Butterworth and Tschebyscheff lowpass characteristics. A plot of $\alpha\,(2\ f_o)$ as a function of filter order (i.e. number of RC sections) is shown in Figure 21. The Butterworth and Tschebyscheff characteristics are far superior to the unloaded - tandem - RC characteristic, and the synthesis of these filters will be briefly discussed in the next section.

3.1.2 Active Lowpass Networks

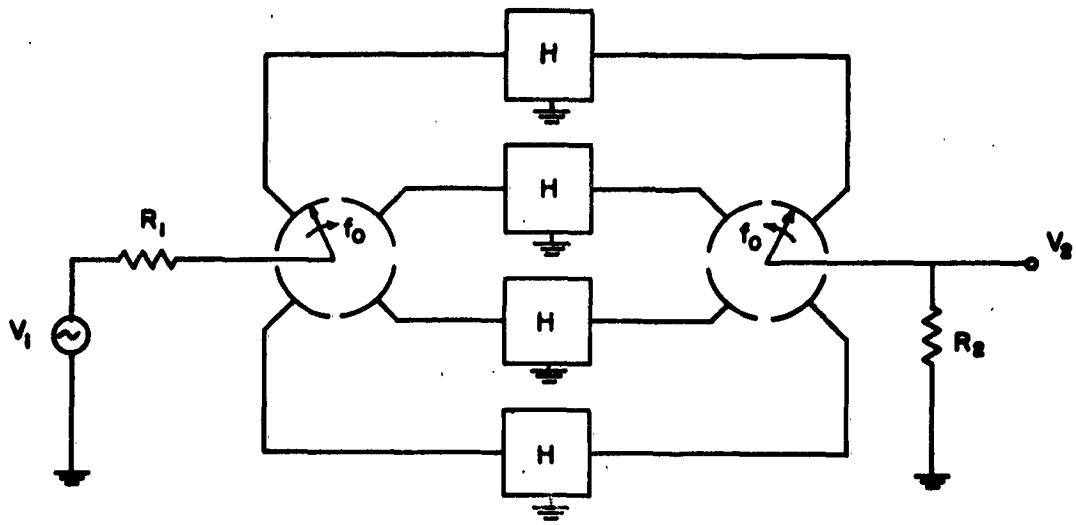
Although passive RC networks can produce poles only along the negative real axis, the complex poles in the Butterworth and Tschebyscheff transfer functions can be achieved with active RC networks. A standard approach in the synthesis of these functions is to write the transfer function as a product of quadratic factors and possibly a linear factor. Each of these factors is realized by an active RC network, and a tandem connection of these networks will then realize the desired transfer function. Thus the transfer function can be written in normalized form as

$$T(S) = \frac{1}{D(S)} = \frac{1}{(S^2 + d_1 S + 1)\text{-------}(S^2 + d_n S + 1)\,(S + 1)}$$

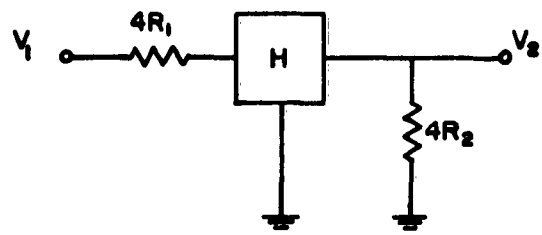
where the term $(S + 1)$ is present only if the denominator polynomial is of odd degree. A proper choice of the d's can produce either a Butterworth or Tschebyscheff characteristic. These coefficients have been tabulated in several places in the literature.(1)

From a practical point of view, the difficulty in generating a particular factor $\dfrac{1}{S^2 + d_i S + 1}$

(1) Sallen and Key: "A Practical Method of Designing RC Active Filters", MIT Lincoln Laboratory Technical Report No. 50.



(a) GENERAL 4-PATH DIGITAL FILTER
(H IS A LOWPASS NETWORK)



(b) EQUIVALENT LOWPASS NETWORK

BASIC DIGITAL FILTER CIRCUIT
FIGURE 21

is related to the magnitude of d_i. As d_i becomes smaller, the tolerances on the active network components must be more stringent. Although the Tschebyscheff response cust off more rapidly than the Butterworth response for a particular polynomial degree, the Tschebyscheff factors contain smaller values of d_i and imply corresponding greater stability problems.

A study of microelectronic realizations of both Butterworth and Tschebyscheff active RC filters will be pursued during the next quarter. These low pass filters will then be assessed for use in a digital filter.

V. CONCLUSIONS

A. DIGITAL DATA TERMINAL AN/TYC-1(XC-2)

Both the Fairchild micrologic elements and the Texas Instruments Solid Circuits are useful in designing the major protion of the Digital Data Terminal. Only the latter circuit family allows, however, a substantial reduction in power consumption of the equipment. It is also felt, that Solid Circuits provide better design flexibility, expecially in non-clocked systems and require in general less components to realize a given function than micrologic elements.

B. TELEGRAPH - TELEPHONE TERMINAL AN/TCC-29

The bandpass characteristic of a digital filter employing simple RC sections in tandem does not possess a sufficiently sharp cut-off characteristic for approximation of the F-316/U bandpass characteristic. However, the use of active RC networks in a digital filter appears to provide a means for an acceptable bandpass characteristic approximation. Further study will determine the feasibility of this approach.

VI. PROGRAM FOR NEXT INTERVAL

The AN/TCC-29 will be studied from a microelectronics system viewpoint in order to determine the impact of microelectronics on such a system. In addition, a study will be conducted to determine the extent to which active RC networks can be used in a digital filter to achieve Butterworth and Tschebyscheff bandpass characteristics which could be useful in a filter of the F-316/U class.

The problem of maintainability for microelectronics systems will be investigated. Analyses will be performed to determine the applicability of replacement, throw-away and repair concepts.

APPROXIMATE ENGINEERING MAN HOURS

During the second quarter, the following manpower was devoted to this contract.

G. Danielson	108 hours
R. Marolf	454 hours
L. Ragonese	40 hours
R. Warr	40 hours
Additional Professional Personnel	136 hours
TOTAL	778 man hours

AD

Electronics Laboratory, General Electric Company Syracuse, New York
SOLID STATE MICROELECTRONIC SYSTEMS by G. Danielson, R. Marolf and R. Warr. Second Quarterly Progress Report - 1 December 1962 to 1 March 1963.
43 pgs. incl. illus. and tables (SC Contract No. DA-36-039-AMC-00020. Unclassified Report

The paper design for the Digital Data Terminal AN/TYC-1(SC-2) has been completed. Detailed logic diagrams for the major portion of the Terminal based on Texas Instruments Solid Circuits and Fairchild micrologic elements are presented.

A microelectronics study for the Telegraph-Telephone Terminal AN/TCC-29 has been initiated. The application of microelectronic techniques to the complete AN/TCC-29 will be studied, but initial efforts have been limited to an evaluation of possible digital filter applications within this equipment. The use of both passive RC and active RC networks within a digital filter is considered.

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